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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/973,019	10/10/2001	Hiroshi Watanabe	214890US2S	5166

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OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VA 22202

EXAMINER
PHAM, HOAI V

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,019	WATANABE ET AL.	
	Examiner	Art Unit	
	Hoai V Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *8-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4* is/are rejected.

7)☒ Claim(s) *3 and 5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a third N-type transistor and a fourth P-type transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

Line 23, "second gate" and "second high" should be changed to --first gate-- and --first high—for clarifying the scope of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kang et al. [U.S. Pat. 5,278,441] previously applied.

Kang et al. (figs. 4-5, cols. 3-4) discloses a semiconductor device, comprising:

a first transistor including a first gate (74) formed on a semiconductor substrate (62), a first low impurity concentration diffusion layer (80, 81) formed on the surface of the semiconductor substrate in a manner to surround the first gate, a first high impurity concentration diffusion layer (89, 90) formed on the surface of the semiconductor substrate in a manner to surround the first low impurity concentration diffusion layer, and a first gate side wall (86) formed to surround the first gate with a top surface of the gate being exposed from an upper end of the first gate side wall, and an interface between the first low impurity concentration diffusion layer and the first high impurity concentration diffusion layer corresponding to a lower and of an outer surface of the first gate side wall; and

a second transistor including a second gate (76) formed on the semiconductor substrate, a second low impurity concentration diffusion layer (83, 84) formed on the surface of the semiconductor substrate in a manner to surround the second gate, a second high impurity concentration diffusion layer (98, 99) formed on the surface of the semiconductor substrate in a manner to surround the second low impurity concentration diffusion layer, and a second gate side wall (86) formed to surround said second gate and having a thickness equal to that of the first gate side wall of the first transistor, a top surface of the second gate being exposed from an upper end of the second gate side wall;

wherein the size of the second low impurity concentration diffusion layer (83, 84) formed on the surface of the semiconductor substrate, which extends from the second gate (76) to reach the second high impurity concentration diffusion layer (98, 99), is larger than the size of the first low impurity concentration diffusion layer (80, 81) formed on the surface of the semiconductor substrate, which extends from the first gate (74) to reach the first high impurity concentration diffusion layer (89, 90), and a lower end of an outer surface of the second gate side wall (86) being positioned within a surface region of the second low impurity concentration diffusion layer and the second high impurity concentration diffusion layer (see fig. 4).

With respect to claim 2, Kang et al. discloses that the first low impurity concentration diffusion layer (80, 81) is an N-type diffusion layer having a low impurity concentration, the first high impurity concentration diffusion layer (89, 90) is an N-type diffusion layer having a high impurity concentration, the first transistor is an N-type transistor, the second low impurity concentration diffusion layer (83, 84) is a P-type diffusion layer having a low impurity concentration, the second low impurity concentration diffusion layer (98, 99) is a P-type diffusion layer having a low impurity concentration, and the second transistor is a P-type transistor (see fig. 4, col. 4, lines 16-68 and col. 5, lines 1-5).

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant Admitted Prior Art (pages 1-11, fig. 22).

Applicant Admitted Prior Art a semiconductor device, comprising:

a first transistor (204) including a first gate (212) formed on a semiconductor substrate (223), a first low impurity concentration diffusion layer (113) formed on the surface of the semiconductor substrate in a manner to surround the first gate, a first high impurity concentration diffusion layer (215) formed on the surface of the semiconductor substrate in a manner to surround the first low impurity concentration diffusion layer, and a first gate side wall (114) formed to surround the first gate with a top surface of the gate being exposed from an upper end of the first gate side wall, and an interface between the first low impurity concentration diffusion layer and the first high impurity concentration diffusion layer corresponding to a lower and of an outer surface of the first gate side wall; and

a second transistor (203) including a second gate (211) formed on the semiconductor substrate, a second low impurity concentration diffusion layer (206)

formed on the surface of the semiconductor substrate in a manner to surround the second gate, a second high impurity concentration diffusion layer (207) formed on the surface of the semiconductor substrate in a manner to surround the second low impurity concentration diffusion layer, and a second gate side wall (111,112) formed to surround said second gate and having a thickness equal to that of the first gate side wall of the first transistor, a top surface of the second gate being exposed from an upper end of the second gate side wall;

wherein the size of the second low impurity concentration diffusion layer (206) formed on the surface of the semiconductor substrate, which extends from the second gate (203) to reach the second high impurity concentration diffusion layer (207), is larger than the size of the first low impurity concentration diffusion layer (113) formed on the surface of the semiconductor substrate, which extends from the first gate (212) to reach the first high impurity concentration diffusion layer (215), and a lower end of an outer surface of the second gate side wall (111,112) being positioned within a surface region of the second low impurity concentration diffusion layer (206) and the second high impurity concentration diffusion layer (207) (see fig. 22).

With respect to claim 4, Applicant Admitted Prior Art discloses that a memory cell transistor (202) including a third gate (200) formed on the semiconductor substrate, a third diffusion layer (214) having a high impurity concentration and formed within the semiconductor substrate around the third gate, and third gate side wall (209b,114) formed around the third gate and having a thickness substantially equal to those of the first and second gate side walls.

Allowable Subject Matt r

7. Claims 3, 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose a third N-type transistor and fourth p-type transistor, wherein the first and second transistors perform the function of a high voltage transistor, and the third and fourth transistors perform the function of a low voltage transistor while having the characteristics as recited in claim 1.

Response to Arguments

9. Applicant's arguments filed 4/10/03 have been fully considered but they are not persuasive.

Applicant argues that the amended claim 1 is not taught or suggest by Kang et al..

Applicant's arguments are not persuasive because Kang et al. discloses all the limitations as recited in claim 1. (see the rejection above)

Applicant argues that the gate side wall 82 of the present invention does not have the lower edge facing the interface of the layers 76a, 76b and 77a, 77b.

Applicant's arguments are not persuasive because there is no basis for this statement.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

11. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V Pham whose telephone number is 703-308-6173. The examiner can normally be reached on 6:30A.M. - 6:00P.M..

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

14. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HP
Hoai Pham
June 12, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800